

IN ADDITION TO THEIR COMMON ROLE AS CLOCK SOURCES IN DIGITAL SYSTEMS, OSCILLATORS PLAY AN IMPORTANT ROLE IN INSTRUMENTATION APPLICATIONS. A SIMPLE AND TUNABLE OSCILLATOR BOOSTS THE PERFORMANCE OF A RANGE OF CIRCUITS. PART 1 OF THIS SERIES PRESENTS AN RTD DIGITIZER, THERMISTOR-TO-FREQUENCY CONVERTERS, AND RELATIVE-HUMIDITY DIGITIZERS.

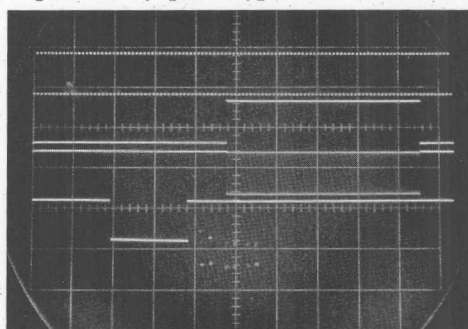
A clock for all reasons, part 1: Monolithic oscillator invigorates instrumentation applications

OSCILLATORS ARE FUNDAMENTAL circuit building blocks. A substantial percentage of electronic apparatus use oscillators as timekeeping references, as clock sources, for excitation, and for other tasks. The most obvious oscillator application is a clock source in digital systems. A second area is instrumentation. Transducer circuitry, carrier-based amplifiers, sine-wave generators, filters, interval generators, and data converters all use forms of oscillators. Although various techniques are common, a simply applied, broadly tunable oscillator with good accuracy widens the design possibilities of many of these circuits.

Commonly employed oscillators are resonant-el-

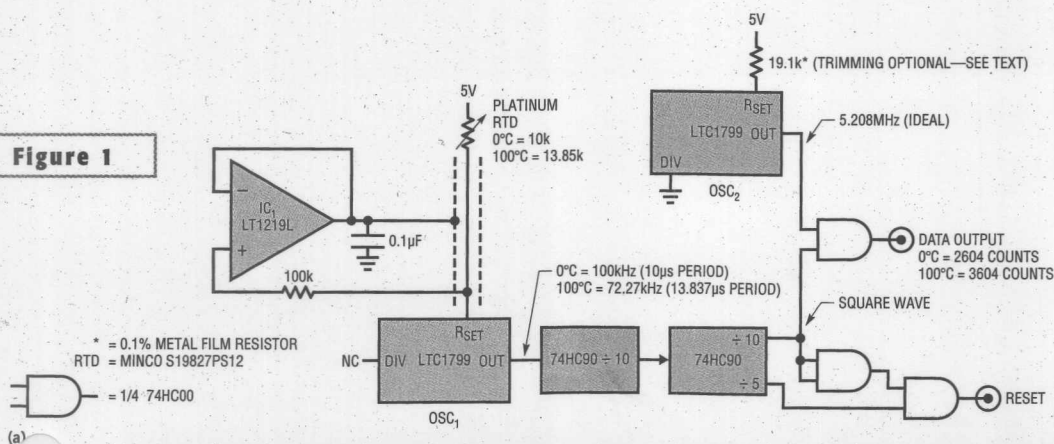
ement based or RC types (Table 1.) Quartz crystals and ceramic resonators offer high initial accuracy and low drift—particularly quartz types—but are

- A (OSC₁ OUTPUT)
- B (SQUARE WAVE)
- C (OUTPUT DATA)
- D (RESET)



HORIZONTAL SCALE=100 μSEC/DIV
VERTICAL SCALE=5V/DIV

Figure 1



A .1um RTD digitizer is accurate to within 1° from 0 to 100°C (a). The circuit divides OSC₁'s output (Trace A) by 100 and gates the result with a 5.2-MHz clock, to produce data bursts (Trace C) that correspond to temperature (b).

essentially not tunable over any significant range. Typical RC types have lower initial accuracy and increased drift but are easily tunable over broad ranges. A problem with conventional RC oscillators is that considerable design effort is necessary to achieve good specifications. The LTC1799 is also an RC type, but its accuracy and drift specifications fit between resonator-based types and typical RC oscillators (see sidebar "A simple, high-performance oscillator"). The device's combination of simplicity, broad tuning range, and good accuracy invites use in instrumentation circuitry, as in the following examples.

PLATINUM RTD DIGITIZER

Using a platinum RTD for R_{SET} of the LTC1799 oscillator results in a highly predictable OSC_1 output period versus temperature (Figure 1a). A series of counters scale the OSC_1 output and present the resultant signal to a clocked, period-determining logic network that delivers digital output data. Over a sensed-temperature range of 0 to 100°C, the circuit delivers 1000 counts with accuracy inside 1°C. You can extend the circuit's range for sensor limits of -50 to +400°C by using a monitoring processor to implement linearity correction in accordance with sensor characteristics. Linearity deviation over -50 to +400°C is several degrees (Reference 1).

If the RTD is at the end of a cable, IC_1 should drive the cable shield, as the figure shows. This action bootstraps the cable shield to the same potential as R_{SET} , eliminating jitter-inducing capacitive-loading effects at the R_{SET} node. The R_{SET} node of the LTC1799 is not unduly sensitive but does require management of stray capacitance (also see sidebar).

Waveforms show the circuit's opera-

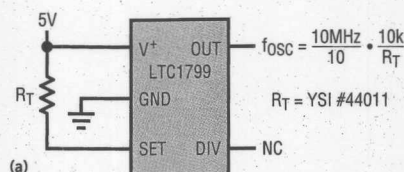
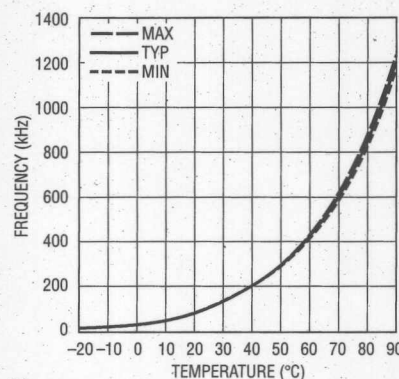


Figure 2



A simple temperature-to-frequency converter uses a thermistor to bias R_{SET} (a) and produces a predictable but nonlinear frequency output (b).

tion (Figure 1b). The RTD determines OSC_1 's output (Trace A), which the circuit divides by 100 and produces in square-wave form (Trace B). The logic network combines with OSC_2 's fixed frequency to digitize the period measurement, which appears as output data bursts (Trace C). The logic also produces a reset output (Trace D), facilitating synchronization of monitoring logic.

The accuracy is approximately 1.5°C, primarily due to the initial error of the LTC1799. Obtaining accuracy inside 1°C involves simulating a temperature of 100°C, which is equivalent to 13,850Ω, at the sensor terminals and trimming R_{SET} for the appropriate output. A precision

resistor decade box, such as the ESI DB62 (www.esi.com), allows convenient calibration.

THERMISTOR-TO-FREQUENCY CONVERTER

A simple circuit also directly converts temperature to digital data (Figure 2a). In this case, a thermistor sensor, R_T , biases the R_{SET} pin. The LTC1799 frequency output is predictable although nonlinear. The inverse R_{SET} -versus-frequency relationship combines with the thermistor's nonlinear characteristic to give Figure 2b's data. The curve is nonlinear although tightly controlled.

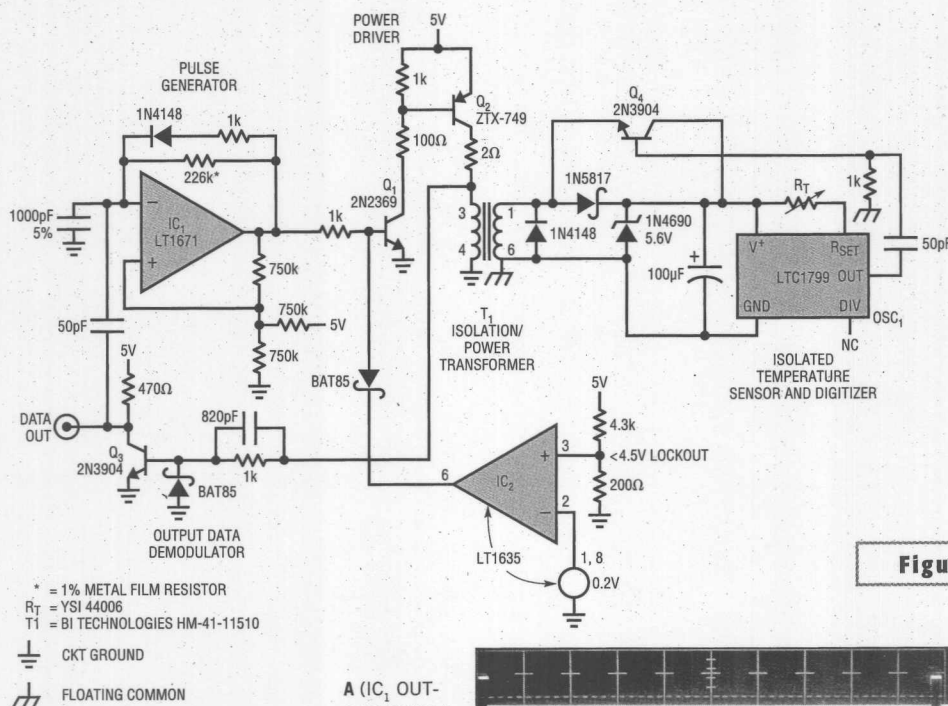
ISOLATED CONVERTER

An alternative circuit, which builds on the previous approach, galvanically isolates the thermistor from the circuit's power and data-output ports (Figure 3a). The 3500V breakdown barrier between the thermistor and the power- and data-output ports permits operation at high common-mode voltages, which are common in industrial-measurement situations.

The pulse generator comprising IC_1 and associated components runs at approximately 10 kHz and produces a 2.5-μsec-wide output Trace A (Figure 3b). Q_1 and Q_2 provide power gain, driving T_1 . (Trace B is Q_2 's collector.) T_1 's secondary responds by charging the 100-μF capacitor to a dc level via the 1N5817 rectifier. The capacitor powers OSC_1 , which oscillates at the sensor-determined frequency. OSC_1 's output, which the circuit differentiates to conserve power, switches Q_4 . Q_4 , in turn, drives T_1 's secondary. T_1 's primary receives Q_4 's signal, and Q_3 amplifies this signal, producing the circuit's data output (Trace C). Q_3 's collector also lightly modulates IC_1 's negative input (Trace D), which synchronizes T_1 's

TABLE 1—CHARACTERISTICS OF OSCILLATOR TYPES

Clock type	Typical frequency accuracy (%)	Typical frequency range	Tunability	Temperature coefficient	Power-supply-rejection ratio	Comments
Quartz	0.005	10 kHz to 200 MHz	Poor	0.5 ppm/°C, easily achieved	1 ppm/V	High stability and initial accuracy at expense of tunability; essentially no tunability; stability of 1×10^{-9} achievable with compensation techniques
Ceramic resonator	0.5	250 kHz to 60 MHz	Poor	30 ppm/°C	20 ppm/V	Lower performance and cost than quartz; essentially untunable
LTC1799	1.5	1 kHz to 33 MHz	Good	40 ppm/°C plus resistor-temperature coefficient	500 ppm/V	Add 10 to 50 ppm/°C temperature coefficient, depending on resistor type; extremely small footprint: SOT-23 and one resistor
Typical RC-based clock	10	1 Hz to 25 MHz	Good	200 ppm/°C	2500 ppm/V	Requires careful design and component selection for best results



(a)

A galvanically isolated thermistor digitizer has a 3500V breakdown barrier (a). IC₁ provides pulsed power (Trace A) to OSC₁ via Q₁, Q₂, and T₁. Q₃ extracts data and presents it to the output (Trace C) (b).

primary drive to the data output. IC₂ prevents erratic circuit operation below 4.5V by removing Q₁'s drive.

The pulse generator's clocking, while maintaining OSC₁'s isolated dc power supply, generates periodic cessations in the frequency-coded output. You can use these interruptions as markers to control

the operation of monitoring logic. Thermistor characteristics determine the output frequency as the Table 2 shows.

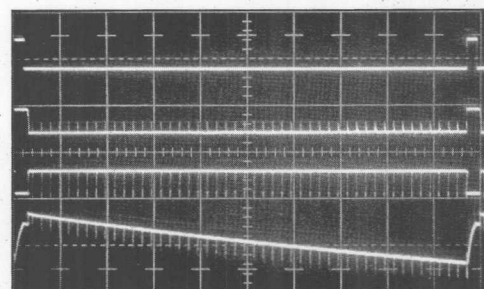
HETERODYNE-BASED RH-SENSOR DIGITIZER

You can also design a circuit to convert the varying capacitance of a linearly responding RH (relative-humidity) sensor

to a frequency output (Figure 4a). The 0-Hz to 1-kHz output corresponds to 0 to 100% sensed RH. Circuit accuracy is 2%, plus an additional tolerance dictated by the selected sensor's grade. Circuit temperature coefficient is 400 ppm/°C, and PSRR (power-supply rejection ratio) is less than 1% over 4.5 to 5.5V. Additionally, one sensor terminal attaches to ground, which is often beneficial for noise rejection.

This circuit is basically a heterodyne circuit. The circuit mixes two oscillators—one variable and one fixed—to produce sum and difference frequencies. The capacitive humidity sensor controls the variable oscillator. The demodulated difference frequency is the output. (Other examples have applied heterodyne techniques, which you usually associate with communications circuitry, to instrumentation. This circuit's operation is adapted from approaches in references 2, 3, and 4.)

Figure 3



(b) HORIZONTAL SCALE=10 μSEC/DIV

frequency-subtraction approach permits a sensed 0% RH to give a 0-Hz output, even though sensor capacitance is not zero at an RH of 0%.

IC₁ and associated components comprise a sensor-controlled variable oscillator that runs between the indicated output frequencies for the noted RH-

A SIMPLE, HIGH-PERFORMANCE OSCILLATOR

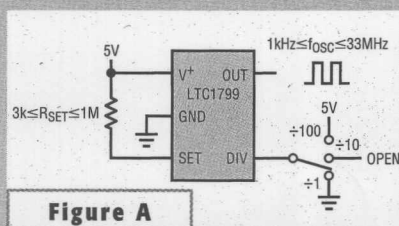
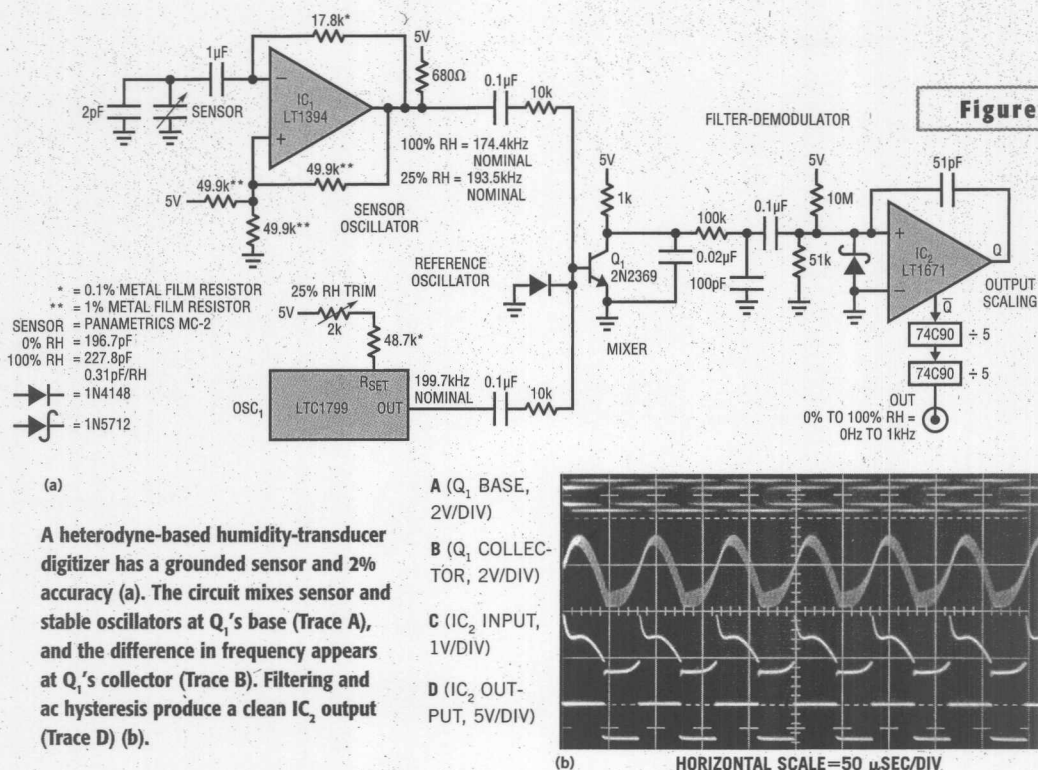


Figure A

The ratio of the voltage between the V⁺ and SET pin and the current entering the SET pin controls the master-oscillator frequency of the LTC1799. A pin-programmable frequency divider permits output-frequency ranging.

The LTC1799 is a simple device with a sole analog input, the R_{SET} node (Figure A). A single R_{SET} resistor at this node programs the device's internal clock, and pin-settable decade dividers scale the output frequency. Various combinations of resistor value and divider choice permit outputs of 1 kHz to 33 MHz. An inverse relationship between resistance and frequency means that the LTC1799's period versus resistance is linear. Its board footprint, a five-pin SOT-23 package and a single resistor, is notably small, and an external timing capacitor is unnecessary.

The ratio of the voltage between the V⁺ and SET pins and the current entering the SET pin controls the device's internal master oscillator. A PMOS transistor and its gate bias force the voltage on the SET pin to approximately 1.13V less than V⁺. This voltage is accurate to ±7% at a particular input current and supply voltage. The effective input resistance is approximately 2 kΩ. The R_{SET} resistor connects internally between the V⁺ and SET pins and locks together the variation between the voltage V⁺ - V_{SET} and current I_{RES}. This design provides the LTC1799's high precision.



sensor excursion. The RH sensor is ac-coupled in accordance with its manufacturer's data sheet; dc coupling introduces destructive electromigration effects (Reference 5). You use the RH trim to tune reference oscillator OSC_1 to IC_1 's nominal 0% RH-dictated frequency. The circuit mixes the two oscillators at Q_1 's base, Trace A (Figure 4b). Q_1 amplifies the mixed-frequency components, although collector filtering attenuates the sum frequency. The RH-determined difference frequency, appearing as a sine wave at Q_1 's collector (Trace B), remains. The circuit filters this waveform and ac-couples the result to zero-crossing detector IC_2 . Hysteretic ac feedback at IC_2 's input (Trace C) produces a clean IC_2 output (Trace D). Counter-based scaling at IC_2 's output combines with slight sensor padding, via the 2-pF value across the sensor, to provide numeric output-frequency correspondence to RH. Calibration involves simulating the RH sensor's 25% value and trimming OSC_1 for a 250-Hz output. You can build the simulated value using known discrete capacitors or simply dial out the value using a precision, variable air capacitor (General Radio 1422D).

When evaluating the circuit's operation, it is useful to consider that the sensor oscillator's frequency changes inversely with sensor capacitance; oscillator

period is linear versus sensor capacitance. This relationship would normally corrupt the desired linear output relationship between frequency and RH. Practically, because the sensor's excursion range is small compared with its 0% RH value, the error is similarly small. This term almost entirely accounts for the circuit's stated 2% accuracy.

CHARGE-PUMP-BASED RH-SENSOR DIGITIZER

A circuit that digitizes the capacitive humidity sensor's output also has better specifications than the previous circuit (Figure 5a). Circuit accuracy is 0.3%, plus the selected sensor grade's tolerance. Temperature coefficient is approximately 300 ppm/ $^{\circ}$ C, and PSRR is 0.25% for $5V \pm 0.5V$. Compromises include a float-

TABLE 2—OUTPUT FREQUENCY VERSUS THERMISTOR CHARACTERISTICS

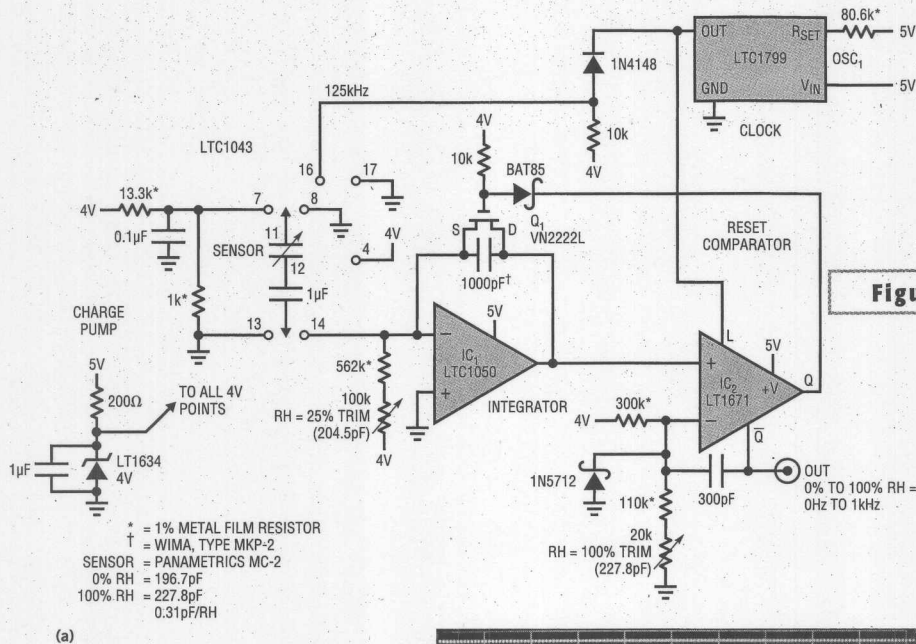
Thermistor value (k Ω)	Sensor temperature ($^{\circ}$ F)	Output frequency
5	109	2.01 MHz
10	77	1.01 kHz
20	47	505 kHz
30	31	337 kHz
40	20	253 kHz
50	12	203 kHz
60	6	168 kHz
70	-1.3	145 kHz
80	-4.7	127 kHz
90	-8.5	113 kHz
100	-12	101 kHz

ing sensor and somewhat more complex circuitry.

OSC_1 (Trace A, Figure 5b) clocks an LTC1043 switch-array-based charge pump. This configuration alternately connects the ac-coupled RH sensor to a 4V-reference-derived potential and then discharges the potential into IC_1 's summing point. IC_1 , an integrator, responds with a ramping output (Trace B). When IC_1 's output exceeds IC_2 's negative input voltage, IC_2 's Q output (Trace C) goes high, triggering Q_1 and resetting the ramp. AC feedback to IC_2 's negative input (Trace D) ensures long enough on-time for

Q_1 to completely reset the ramp. This action's repetition rate depends on the RH sensor's value. OSC_1 's output path to IC_2 's latch input synchronizes the IC_1 - IC_2 loop to the charge pump's clocking. In theory, if the charge pump, the offset term (25% trim current), and the ramp amplitude tie to the same potential, this circuit does not require a voltage reference. In practice, the sensor's extremely small capacitance shifts magnify the effect of charge-pump errors versus the supply, necessitating powering the LTC1043 from the 4V reference, which effectively ties all of these points to the 4V reference. Note that the 5V-powered OSC_1 output requires level shifting to drive the LTC1043.

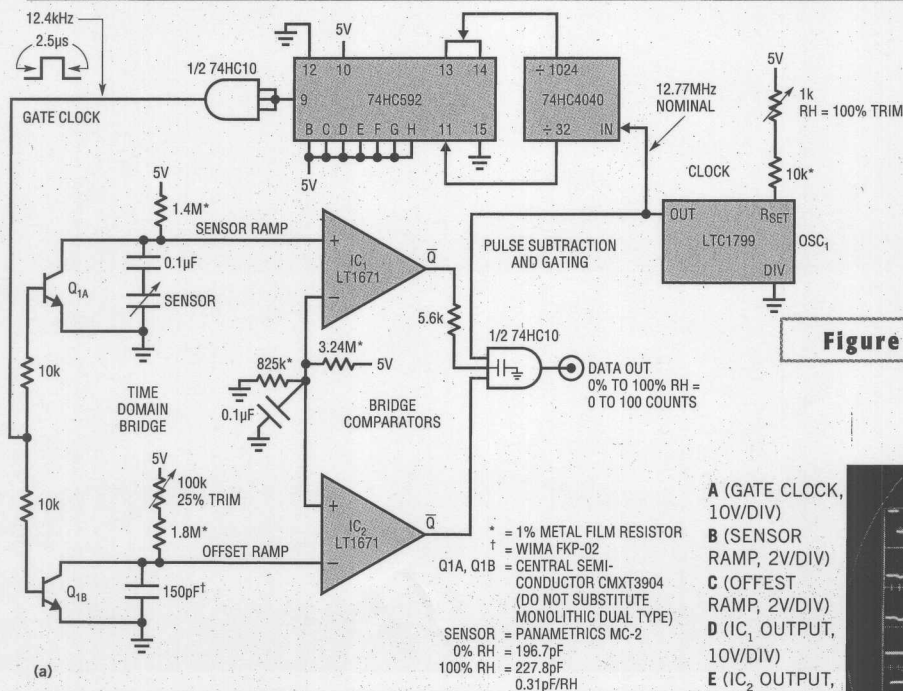
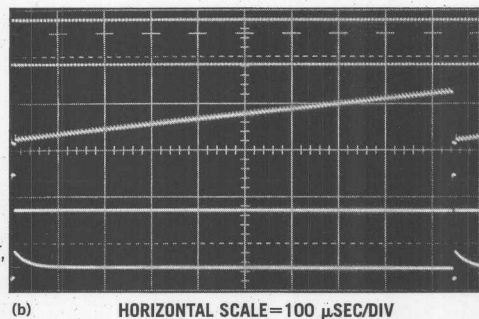
A trimmed dc-offset current, via the 100-k Ω potentiometer, into IC_1 's summing junction compensates the RH sensor's offset term (without compensation 0% RH $\neq$ 0 pF). The 20-k Ω trim at IC_2 scales the output frequency so that 0 to 100% RH equates to a range of 0 to 1 kHz. Trimming involves substituting capacitance for the sensor's known 100 and 25% values and trimming the appropriate adjustments. The adjustments are somewhat interactive, necessitating repetition until convergence occurs. A precision variable capacitor (General Radio type 1422D) is invaluable in this regard, although you can achieve acceptable re-



(a)

A hygrometer digitizer has 0.3% accuracy, but the sensor must float off-ground (a). OSC_1 drives an RH-sensor-based charge pump, producing a ramp at IC_1 (Trace B). IC_2 's Q output biases Q_1 to reset the ramp (Trace C), and the frequency output at $\bar{Q}$ varies with humidity (b).

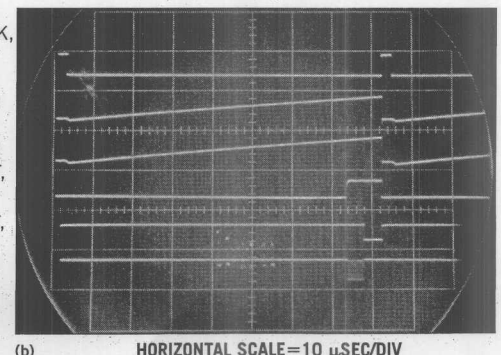
- A (OSC_1 OUTPUT, 5V/DIV)
- B (IC_1 OUTPUT, 1V/DIV)
- C (IC_2 Q OUTPUT, 5V/DIV)
- D (IC_2 -INPUT, 5V/DIV)



(a)

A humidity-transducer digitizer has a grounded sensor and 1% accuracy (a). Q_{1A} and Q_{1B} produce ramp outputs (Traces B and C), and IC_1 and IC_2 digitize the ramp times (Traces D and E). The digitized output consists of 0 to 100 counts for 0 to 100% RH (Trace F) (b).

- A (GATE CLOCK, 10V/DIV)
- B (SENSOR RAMP, 2V/DIV)
- C (OFFSET RAMP, 2V/DIV)
- D (IC_1 OUTPUT, 10V/DIV)
- E (IC_2 OUTPUT, 10V/DIV)
- F (DIGITIZED OUTPUT, 10V/DIV)



(b)

sults with built-up calibrated discrete capacitors.

RH-SENSOR DIGITIZER

Another RH digitizer features 1% accuracy, PSRR of 1% over 4.5 to 5.5V, temperature coefficient of 350 ppm/°C, and a ground-referred sensor (Figure 6a). Additionally, the circuit's trim scheme accommodates RH sensors with a wide tolerance grade. The circuit is basically a time-domain bridge; it subtracts time intervals representing sensor and sensor-offset values to determine the sensor value extrapolated to RH=0%. This measurement is digitized and scaled so that 0 to 100 counts corresponds to 0 to 100% RH at the output.

OSC_1 's nominal 12.77-MHz output, which the circuit conditions using a counter chain and an inverter-configured gate, presents a 12.4-kHz, 2.5-µsec pulse, Trace A (Figure 6b), to Q_{1A} and Q_{1B} . The transistors' collectors fall to 0V. (Trace B is Q_{1A} 's collector, Trace C is Q_{1B} 's collector.) When the base drive ceases, both collectors ramp toward 5V. The slope of Trace B's ramp varies with the RH sensor's capacitance; the slope of Trace C's ramp represents the sensor's offset value (0% RH ≠ 0 pF). IC_1 and IC_2 switch when their associated ramp inputs cross the comparators' common dc-input potential. The comparator outputs (Trace D = IC_1 , Trace E = IC_2) define a "both-high" time region proportional to the ramp slopes' difference and, hence, an offset-corrected version of the sensor's value. The circuit gates this time interval with OSC_1 's output to provide the data output (Trace F).

Circuit operation is fairly straightforward, although some details bear

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designfeature

mention. Q_1 , a dual transistor, promotes cancellation of the individual transistors' V_{CE} -versus-temperature terms, minimizing their error contribution. Q_1 's transistor is a two-die type to minimize crosstalk; do not substitute monolithic types. Similarly, do not substitute a dual comparator for the single types of IC_1 and IC_2 . Also, the comparators operate at high source impedance relative to their input characteristics, but symmetry provides adequate error cancellation. Finally, the 5.6-k Ω resistor combines with the output gates' input capacitances, forming a lag of approximately 20 nsec. This delay prevents false output-data transients when the ramps are resetting.

The trimming procedure is similar to that of the previous RH circuit. Trimming involves substituting capacitance for the sensor's known 100 and 25% values and trimming the indicated adjustments. The adjustments are somewhat interactive, necessitating repetition until convergence occurs. As with the previous circuits, a precision variable capacitor (General Radio type 1422D) is invaluable for this work, although acceptable results are possible with calibrated discrete-capacitor assemblies. □

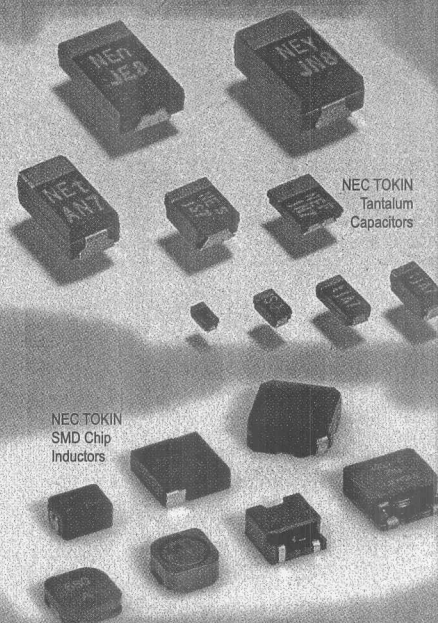
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AUTHOR'S BIOGRAPHY

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge). Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

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PART 1 OF THIS SERIES PRESENTED A VARIETY OF CIRCUITS THAT USE A MONOLITHIC OSCILLATOR IN VARIOUS APPLICATIONS. PART 2 CONTINUES WITH MORE EXAMPLES: CHOPPED AMPLIFIERS, SINE-WAVE GENERATORS, AN INTERVAL GENERATOR, AND AN ADC.

A clock for all reasons, part 2: Monolithic oscillator invigorates instrumentation applications

ALTHOUGH THE MOST OBVIOUS APPLICATION for an oscillator is as a clock source in digital systems, a second application area is instrumentation. A variety of circuits, continued here from part 1 of this series, which appeared in *EDN's* June 26 issue, attests to the usefulness of a simple and accurate monolithic oscillator.

CHOPPED BIPOLAR AMPLIFIER

An adaptation of a previous circuit (**Reference 1**) combines a low-noise op amp with a chopper-based carrier-modulation scheme to achieve an extraordinarily low-noise, low-drift dc amplifier (**Figure 1a**). The dc drift and noise performance exceed any currently available monolithic amplifier. Offset is in-

side 1 μV with drift less than 0.05 $\mu\text{V}/^\circ\text{C}$. Noise in a 10-Hz bandwidth is less than 40 nV, far below monolithic chopper-stabilized amplifiers. Bias current, set by the bipolar LT1028 op amp's input, is approximately 25 nA. One 5V supply powers the circuit, although its output swings $\pm 2.5\text{V}$. Additionally, a carefully selected chopping frequency prevents deleterious interaction with 60-Hz related components at the amplifier's input. These specifications suit demanding transducer-signal-conditioning sit-

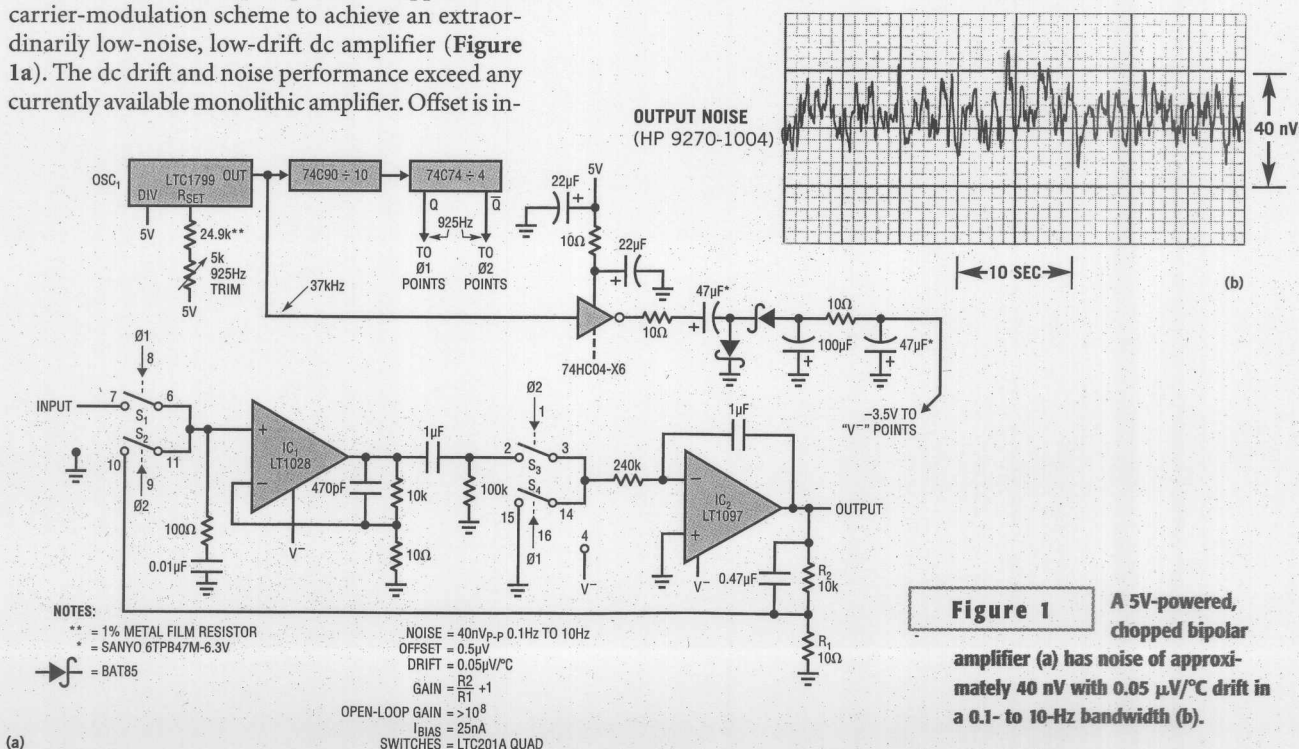
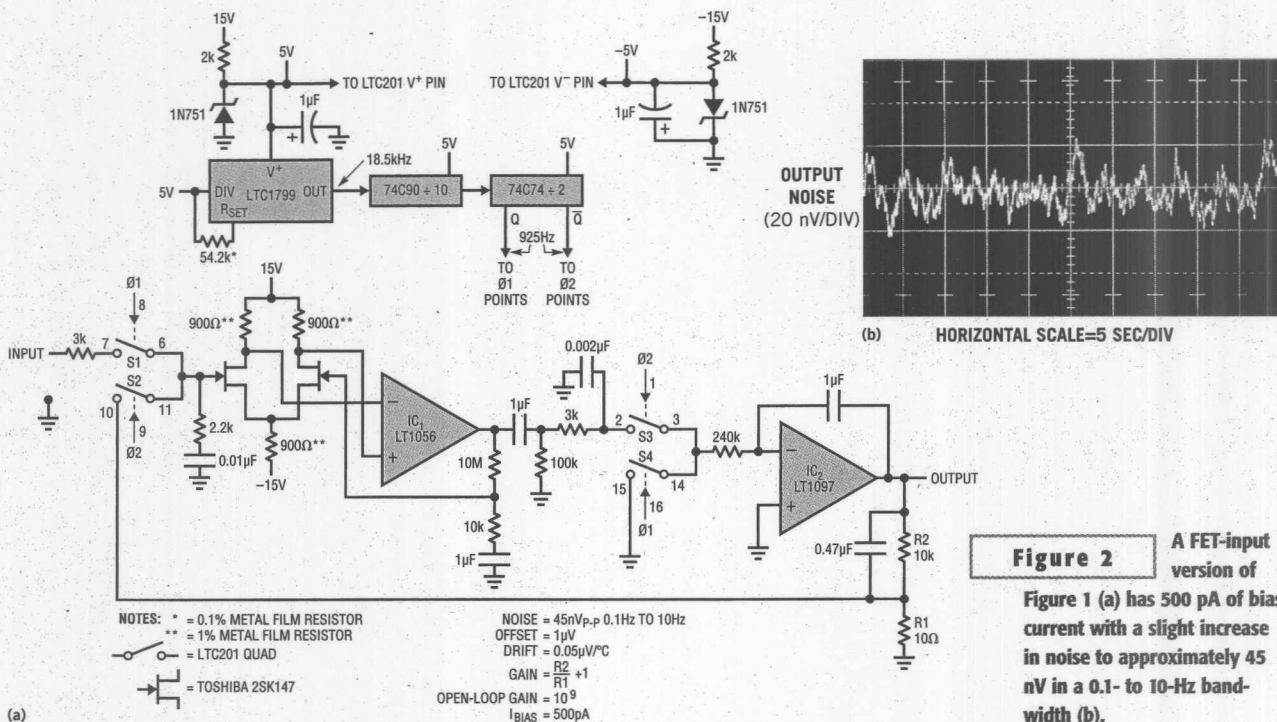


Figure 1 A 5V-powered, chopped bipolar amplifier (a) has noise of approximately 40 nV with 0.05 $\mu\text{V}/^\circ\text{C}$ drift in a 0.1- to 10-Hz bandwidth (b).



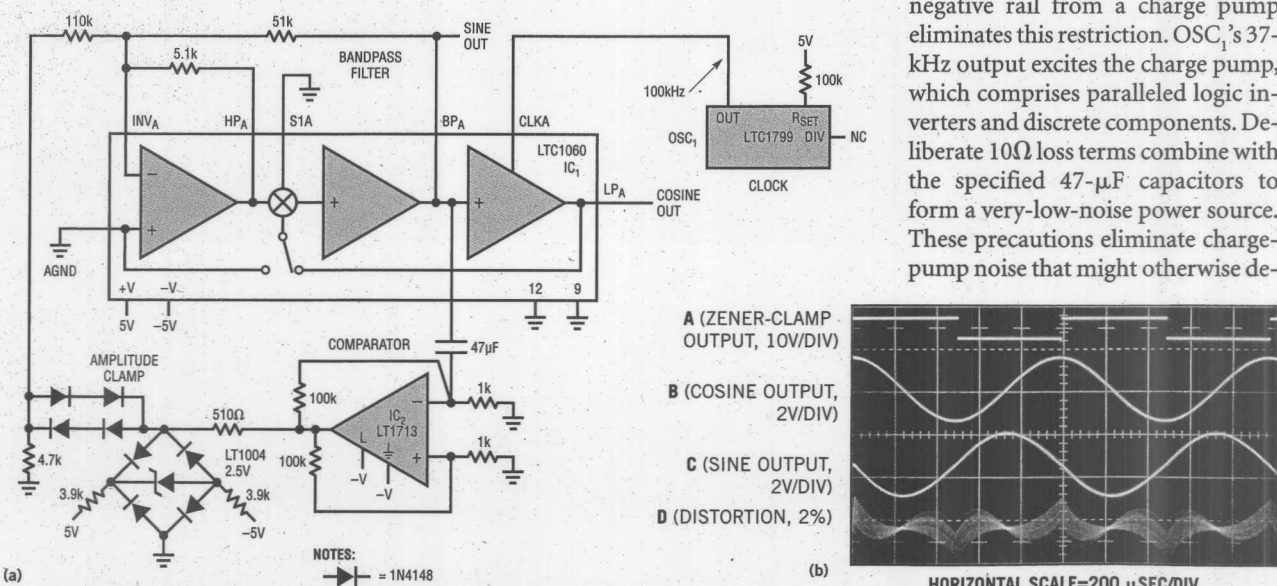
uations, such as high-resolution scales and magnetic search coils.

The circuit divides OSC₁'s 37-kHz output to form a two-phase, 925-Hz square-wave clock. This frequency, harmonically unrelated to 60 Hz, provides excellent immunity to harmonic beating or mixing effects, which could cause instabilities. S₁ and S₂ receive complementary drive, causing IC₁ to see a chopped version of the input voltage. IC₁ amplifies

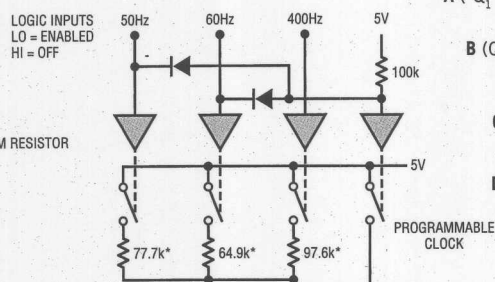
this ac signal. S₃ and S₄ synchronously demodulate IC₁'s square-wave output. Because the input chopper synchronously drives these switches, the circuit presents the proper amplitude and polarity information to IC₂, the dc output amplifier. This stage integrates the square wave into a dc voltage, providing the output. The circuit divides down the output via R₂ and R₁ and feeds back the result to the input chopper where the feedback signal

serves as a zero-signal reference. The R₁-to-R₂ ratio sets the gain, which is 1000 in this case. Because IC₁ is ac-coupled, its dc offset and drift do not affect overall circuit offset, resulting in the extremely low offset and drift performance. IC₂'s input damper minimizes offset-voltage contribution due to nonideal switch behavior.

Normally, this single-supply amplifier's output would be unable to swing to ground. However, powering the circuit's negative rail from a charge pump eliminates this restriction. OSC₁'s 37-kHz output excites the charge pump, which comprises paralleled logic inverters and discrete components. Deliberate 10 Ω loss terms combine with the specified 47- μ F capacitors to form a very-low-noise power source. These precautions eliminate charge-pump noise that might otherwise de-



NOTES:
 * = 0.1% METAL FILM RESISTOR
 $\rightarrow$ = 1N4148
 SWITCHES = LTC201
 ($\rightarrow$) =

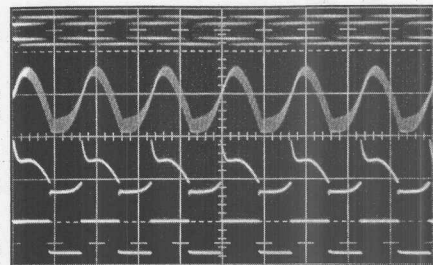


A (Q₁ BASE, 2V/DIV)

B (Q₁ COLLECTOR, 2V/DIV)

C (IC₂ +INPUT, 1V/DIV)

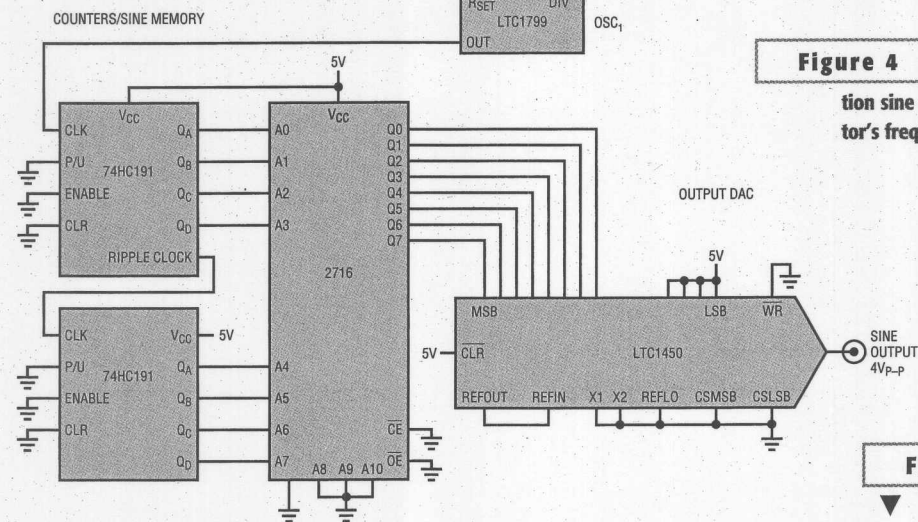
D (IC₂ OUTPUT, 5V/DIV)



(b) HORIZONTAL SCALE=50 μSEC/DIV

Figure 4

A counter-driven, sine-encoded memory produces a 0.75%-distortion sine wave via a DAC. The LTC1799 oscillator's frequency sets the output frequency.



(a)

Clock-related products are evident in the distortion presentation of Figure 4's sine output (a). Fast oscillator-frequency shifting permits crisp changes in the output sine wave's frequency (b). The sine wave's amplitude

Figure 5

instantaneously and faithfully responds to the DAC-reference input step (c).

grade amplifier-noise performance.

A noise plot of the amplifier in a 0.1- to 10-Hz bandwidth shows approximately 40 nV of peak-to-peak noise (Figure 1b). IC₁ and the 60Ω resistance of the S₁-S₂ pair contribute approximately equally to form this noise. When using this amplifier, it is important to realize that IC₁'s bias current flowing through the input source impedance causes additional noise. In general, to maintain low-noise performance, the design should keep the source resistance at less than 500Ω. Fortunately, the output resistances of transducers, such as strain-gauge bridges, RTDs, and magnetic detectors, are well below this resistance figure.

CHOPPED FET AMPLIFIER

You can replace the previous circuit's input stage with a pair of extremely low-noise J-FETs to achieve noteworthy noise performance for a FET-input amplifier (Figure 2a). In most other respects, circuit operation is similar to that of the circuit in Figure 1a. Noise increases slightly to approximately 45 nV, but bias current decreases to 500 pA, which is 50 times lower than the previous circuit. The noise performance is noteworthy because it is almost 17 times better than

currently available monolithic chopper-stabilized amplifiers and nearly equals the best bipolar designs. Other performance specifications, appearing in Figure 2a, are similar to those in Figure 1a.

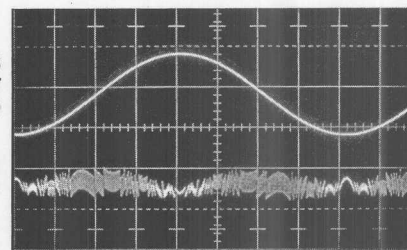
This circuit retains the 925-Hz clock, although this ±15V-powered design uses zener diodes to derive internal ±5V points. The clock and logic run from 5V, and the LTC201 switches use ±5V. The switches' low-voltage rails reduce charge injection, minimizing its effect on offset voltage. RC damper networks further attenuate parasitic switch-behavior effects, resulting in the 1-μV offset specification.

Noise measured over a 50-sec interval is approximately 45 nV in a 0.1- to 10-Hz bandwidth (Figure 2b). This noise is spectacularly low for a J-FET based design and is directly attributable to the input pairs' die size and current density (references 2 and 3).

FIGURE 4'S
SINE OUTPUT
(2V/DIV)

DISTORTION
(0.75%)

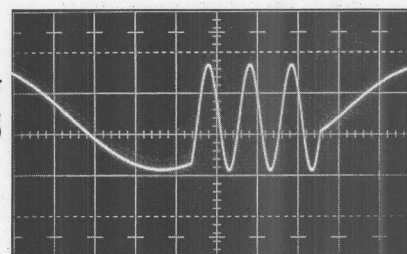
(a)



HORIZONTAL SCALE=2 mSEC/DIV

SINE OUTPUT
(1V/DIV,
UNCALIBRATED)

(b)

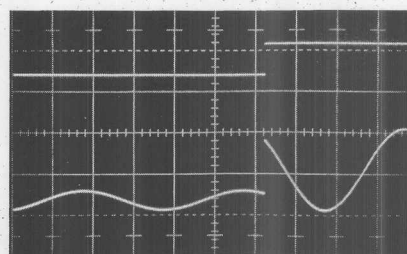


HORIZONTAL SCALE=2.5 mSEC/DIV

DAC-
REFERENCE
INPUT STEP
(2V/DIV)

SINE OUTPUT
(2V/DIV)

(c)



HORIZONTAL SCALE=5 mSEC/DIV

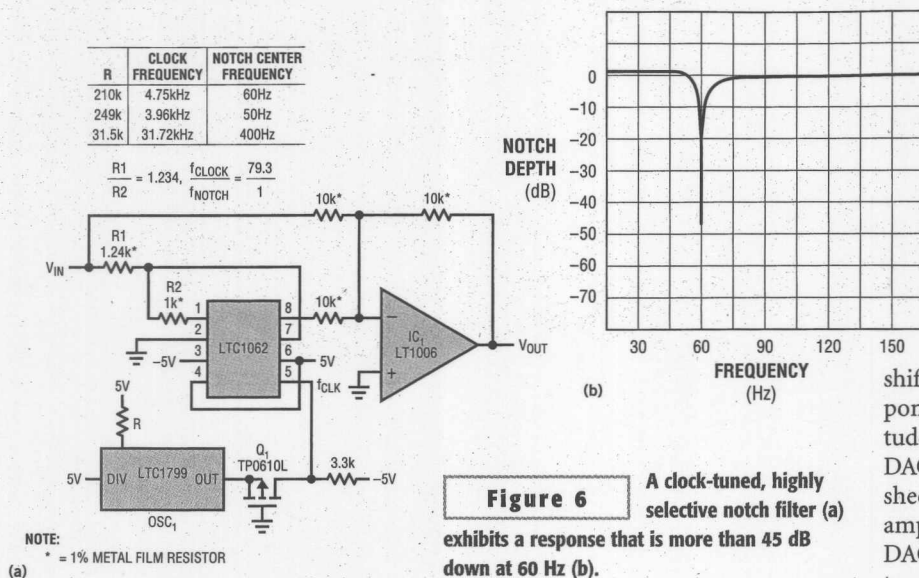


Figure 6 A clock-tuned, highly selective notch filter (a) exhibits a response that is more than 45 dB down at 60 Hz (b).

A sine-wave generator takes advantage of the fact that you can purposely design a feedback-loop-enclosed resonator that oscillates (Figure 3a). This circuit eliminates the need for an amplitude-control loop. This circuit, a mildly modified form of the Regan resonant-bandpass loop, is clock-tunable and produces sine and cosine outputs (Reference 4).

The circuit sets up IC₁'s switched-capacitor filter as a clock-tunable bandpass filter with a Q of 10. OSC₁ clocks the filter at 100 kHz, resulting in a 1-kHz bandpass. The sine output switches IC₂, which supplies square-wave drive to the filter input in regenerative fashion. The loop is self-sustaining, resulting in continuous sine-wave outputs at the indicated points. Zener-bridge clamping of IC₂'s output stabilizes the square-wave amplitude that the circuit applies to the filter and, hence, stabilizes the sine-wave outputs. This form of amplitude control eliminates AGC loop-settling times and potential in-

stabilities. Changes in OSC₁'s clock frequency permit bandpass tuning with no amplitude shifts during or after tuning.

The bandpass filter, responding to IC₂'s clamped output (Trace A, Figure 3b), produces sine (Trace C) and cosine (Trace B) outputs (Figure 3b). Distortion (Trace D), which filter-clock residue dominates, is 2%.

The continuous clocking of a sine-coded look-up-table memory generates a variable-frequency sine wave (Figure 4). A DAC converts the memory's state to an analog output. The strength of this technique is its rapid, high-fidelity response to frequency- and amplitude-change commands. OSC₁'s output, which digital-control inputs set to one of three output frequencies, clocks the 74HC191 counters. These counters parallel load a 2716 EPROM programmed to produce an 8-bit (256 states) digitally coded sine wave (For a copy of the sine-wave-generation code, see the Web version of this

article at www.edn.com.)

The circuit in Figure 4 tunes the sine-wave output in this case to 60 Hz (Trace A, Figure 5a). Distortion mostly comprises clock residue and measures approximately 0.75% (Trace B). The digital inputs abruptly change the output frequency to 400 Hz and then promptly return it to 60 Hz (Figure 5b). These frequency shifts occur crisply, with no alien components or untoward behavior. Amplitude shifts, accomplished by driving the DAC's reference input (see LTC1450 data sheet), are similarly well-behaved. The amplitude faithfully responds to the DAC-reference input step (Figure 5c, traces B and A, respectively). As before, the lack of control-loop time constants promotes the uncorrupted response.

A quick, clean way to tune a notch filter's center frequency is by varying a single, switchable resistor (Figure 6a). The LTC1062 switched-capacitor filter and LT1006 amplifier form a clock-tunable notch. OSC₁, running from the 5V supply, furnishes the clock, which Q₁ level-shifts to drive the $\pm 5V$ -powered LTC1062. The table in the figure shows three common notch frequencies; you can select others by tuning OSC₁ using the equations in the figure.

The filter's performance at a 60-Hz center frequency shows that the response is down more than 45 dB, with steep slopes on either side of the notch (Figure 6b). The circuit maintains this characteristic over broad ranges of the clock-tuned center frequency.

An accurate interval generator, or "one shot," with a large dynamic range includes a clock, a counter, and a dual flip-

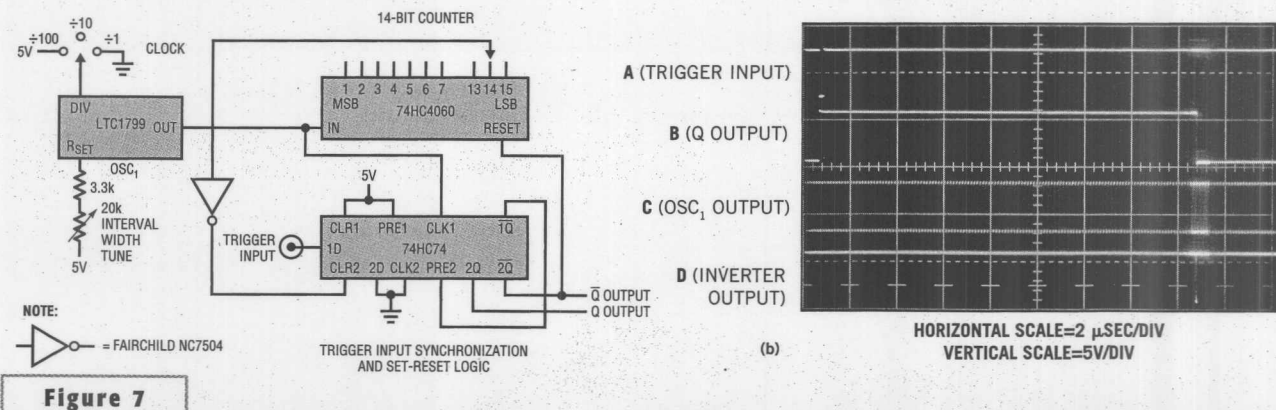


Figure 7

A 1%-accurate interval generator has a dynamic range of 20×10^6 to 1 (a). The trigger-input pulse (b, Trace A) sets the circuit's Q output high (Trace B), and the LTC1799 oscillator (Trace C) clocks the counter until the counter output-biases the inverter low to reset the circuit output (Trace D).

flip (Figure 7a). The clock frequency and counter modulo are programmable. A trigger input passes to the flip-flop IC's $\overline{1Q}$ output (Trace A, Figure 7b) synchronously with OSC_1 's clock (Trace C). This output going low sets the 2Q output—the same as the circuit's Q output—high (Trace B). Simultaneously, the $\overline{2Q}$ output resets the 4060 counter, allowing it to accumulate clock pulses (Trace C, Figure 7b). When enough clock pulses occur to set the selected 4060 output high, the flip-flop IC's CLR2 clear input (Trace D) goes low, ending the circuit's output width. OSC_1 's frequency and the counter's modulo, which are both variable over many decades, set the output width. In Figure 7a's circuit, the interval is programmable from 800 nsec to 16 sec, although other counters can extend this range. Interval accuracy and stability almost entirely depend on OSC_1 's programming resistor.

8-BIT, 80- μ SEC. PASSIVE-INPUT ADC

In general, monolithic ADCs have replaced discrete types. Occasionally, specific desirable circuit characteristics dictate a discrete design. Examples of such special cases include the need for a passive analog input, a particular output data format or control protocol, and economic constraints. An 8-bit design has 90-ppm/°C drift (less than 1 LSB at 0 to 70°C) and converts in 80 μ sec (**Figure 8a**). The circuit, a modern incarnation of an early electronic ADC, consists of a current source, an integrating capacitor, a comparator, logic, and a clock (**Reference 5**).

Applying a pulse to the convert-command input causes the flip-flop's 1Q output to go high (Trace A) when OSC,

clocks the CLK₁ input (**Figure 8b**). This action turns on Q₃, resetting the 0.01-μF capacitor (Trace B). Simultaneously, the flip-flop's $\overline{1Q}$ output goes low, pulling the CLK₂ and CLR₂ inputs down. IC₁'s Q output, which is the circuit's status output (Trace C), also goes low, and IC₁'s $\overline{Q}$ output rises high. This logic state prevents any of OSC₁'s clock pulses from transmitting to the circuit's data output (Trace D). When the convert command falls, the flip-flop's 1Q output goes low, Q₃ turns off, and the 0.01-μF capacitor's voltage begins to ramp. Concurrently, $\overline{1Q}$ goes high, allowing clock pulses to appear at the data output. When the ramp crosses the voltage at E_{IN}, IC₁'s outputs exchange state, pulling the CLK₂ and CLR₂ lines low, and data-output pulses cease. Thus, the OSC₁-originated clock burst appearing at the data output is directly and solely proportional to E_{IN}. For the arrangement in **Figure 8a**, 256 pulses appear for a 2V full-scale input. Conversion time decreases with the time required for the ramp to cross E_{IN}. A full-scale conversion requires 80 μsec, linearly descending to 8 μsec at 0.1 scale.

The circuit connects the second flip-flop in the 74HC74 as a logic buffer that duplicates the high-impedance diode and 2-k Ω resistor node's logic state. Thus, you should minimize this node's trace capacitance, which this design accomplishes by locating the diodes and 2-k Ω resistor adjacent to the CLK2 and CLR2 inputs. You can trim the circuit by applying a 2V input and

adjusting OSC₁'s frequency output using the 5-k Ω calibrating potentiometer for 256 data-output pulses per conversion. $\square$

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AUTHOR'S BIOGRAPHY

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge).

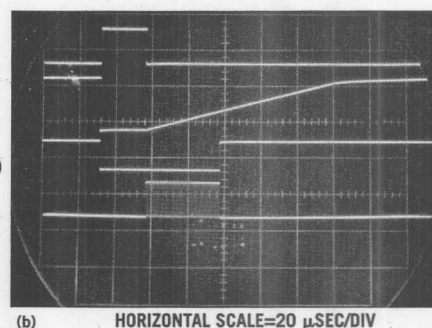
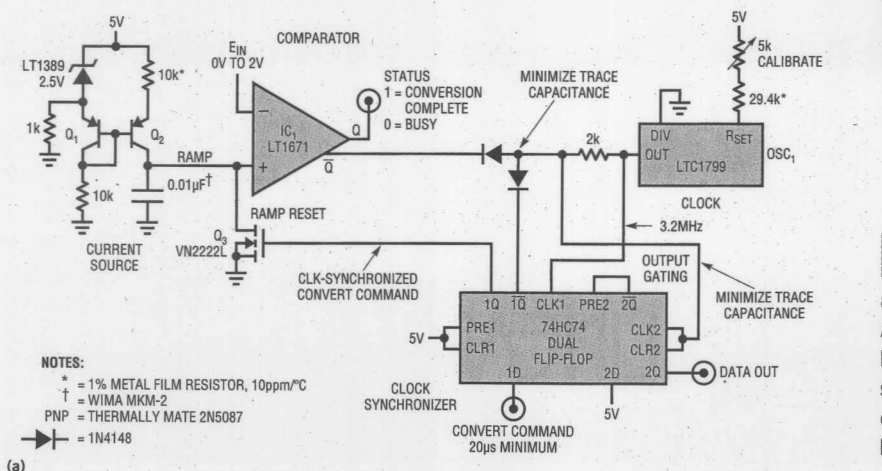


Figure 8 A simple 8-bit ADC has a passive, high-impedance input and an 80- μ sec conversion time (a). A synchronized convert command (b, Trace A) begins a reference ramp and forces the circuit status output low (Trace C). When the ramp crosses E_{IN} 's voltage, the circuit output's clock burst ceases (Trace D).